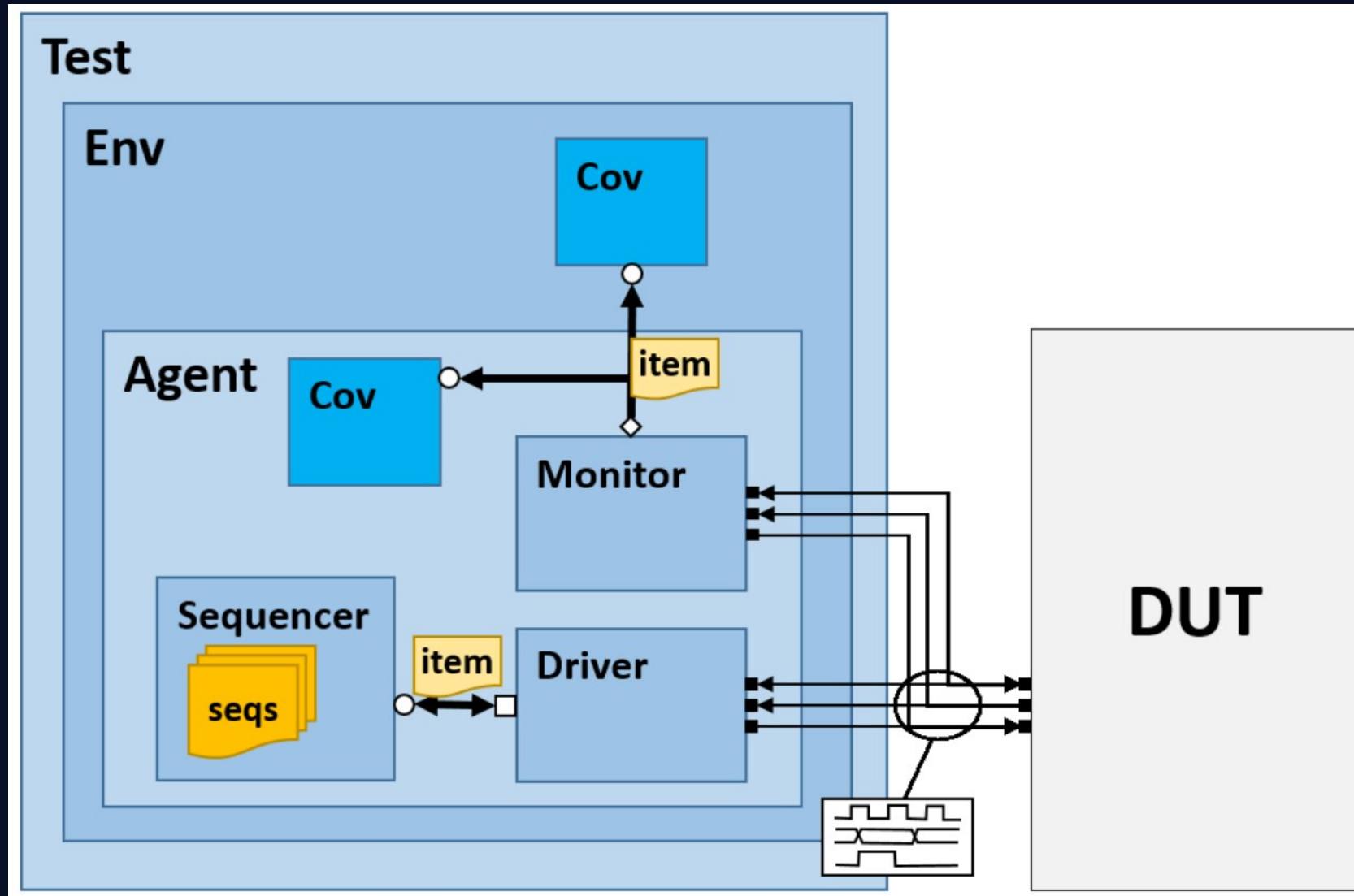


UVM Verification Methodology



Demo Session

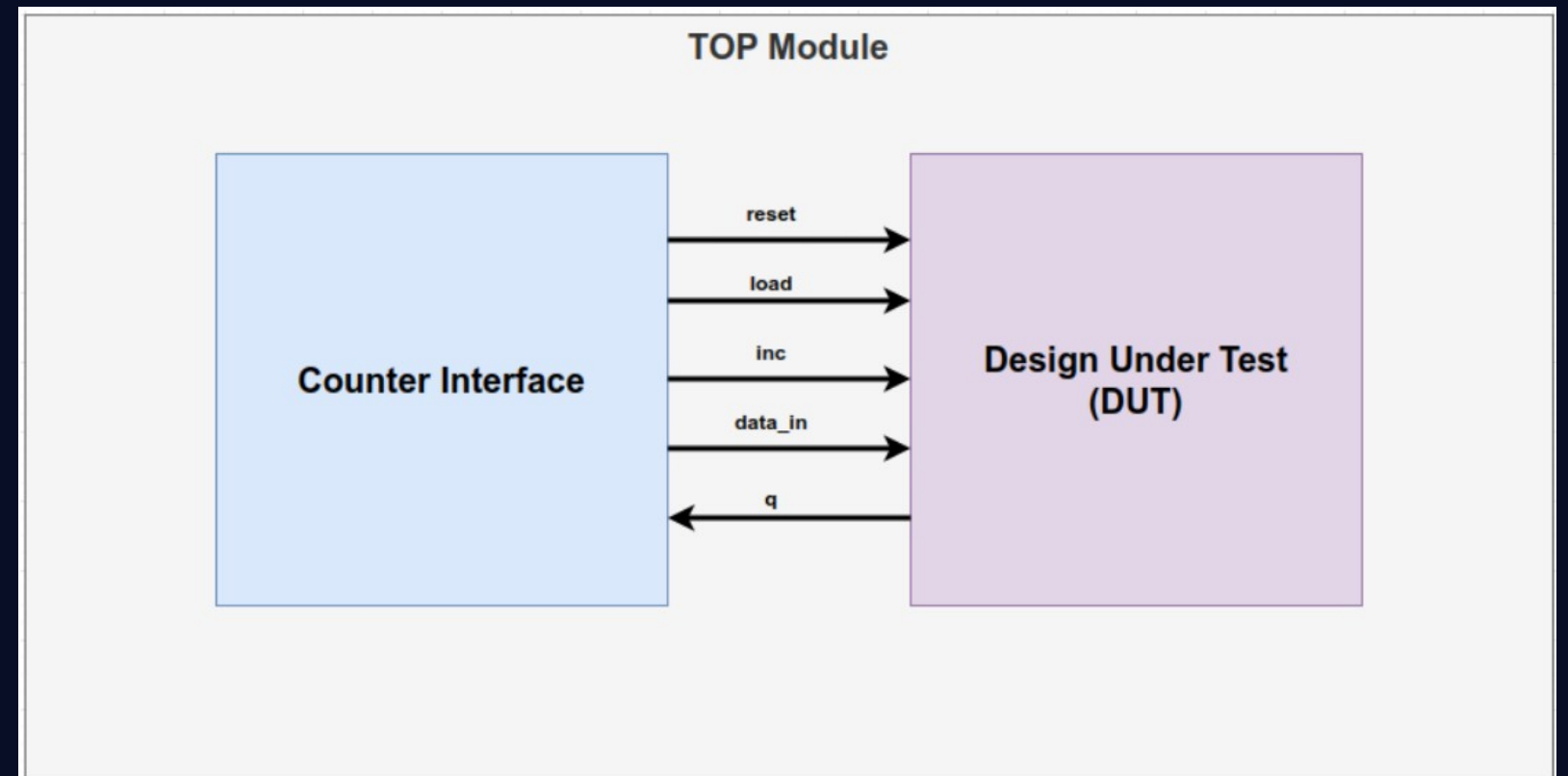
Top Module in UVM Testbench

Overview

- Central integration point of the UVM testbench
- Connects DUT, interface, and all UVM components
- Responsible for simulation start (run_test()) and configuration

Key Components

- Interface
- DUT (8-bit Counter Example)



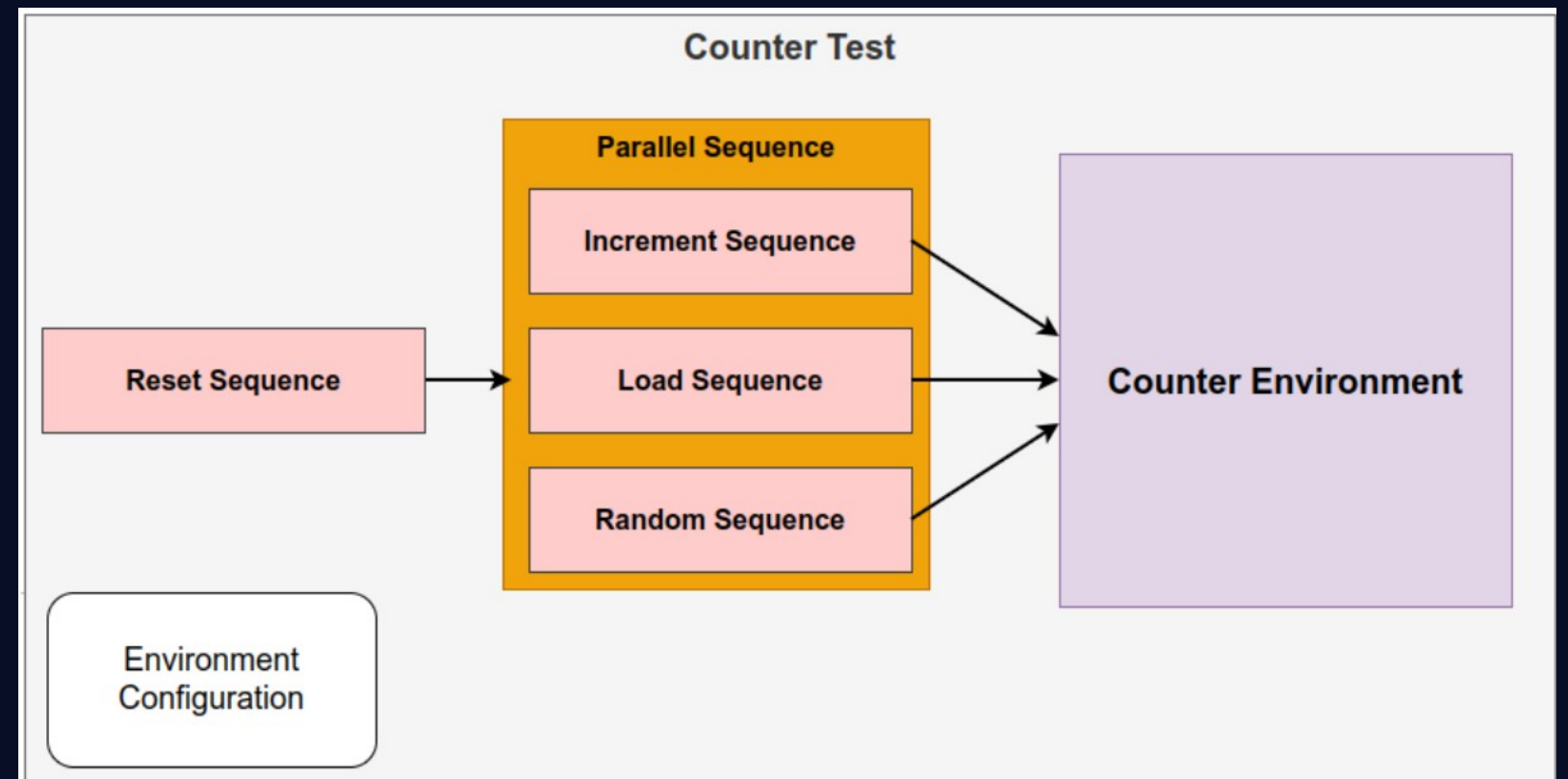
UVM Test in UVM Testbench

Overview

- Acts as central control unit for testbench execution
- Responsibilities:
 - Instantiate environment
 - Configure components
 - Control sequences & test scenarios
- Defines high-level stimulus for DUT

Key Components

- Environment (Agents, Driver, Monitor, Sequencer)
- Test Sequences



UVM Sequence Item & Sequences

UVM Sequence Item Overview

- Represents a transaction between testbench and DUT
- Encapsulates stimulus + response data
- Built-in features: randomization, print, copy, compare

UVM Sequences Overview

- Ordered set of sequence items (transactions)
- Supports sequential & parallel execution

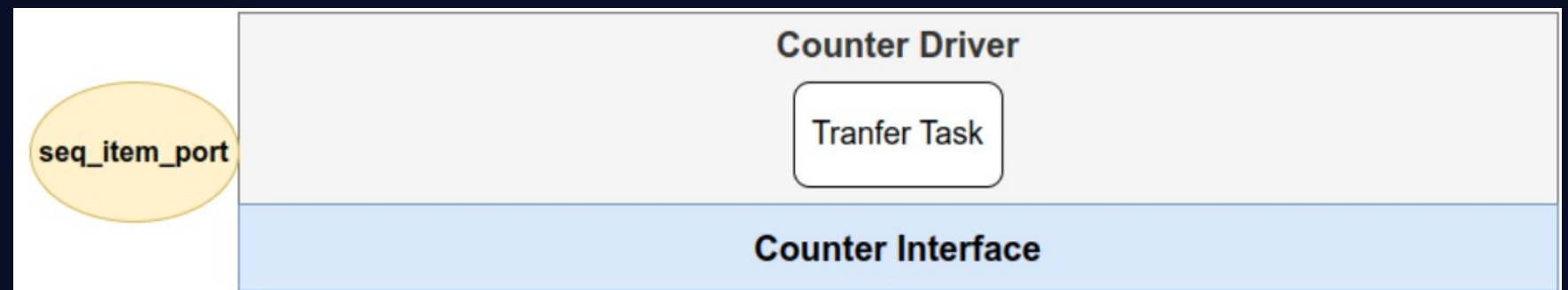
Counter Sequences Overview

- Reset Sequence: Initialize counter to 0
- Increment Sequence: Repeated increments
- Load Sequence: Load random values
- Random Sequence: Random data + op

UVM Driver in UVM Testbench

Overview

- Core component that drives transactions to the DUT
- Converts sequence items → signal-level activity
- Interfaces with DUT via virtual interface



Key Components

- Interface
- Sequence Item

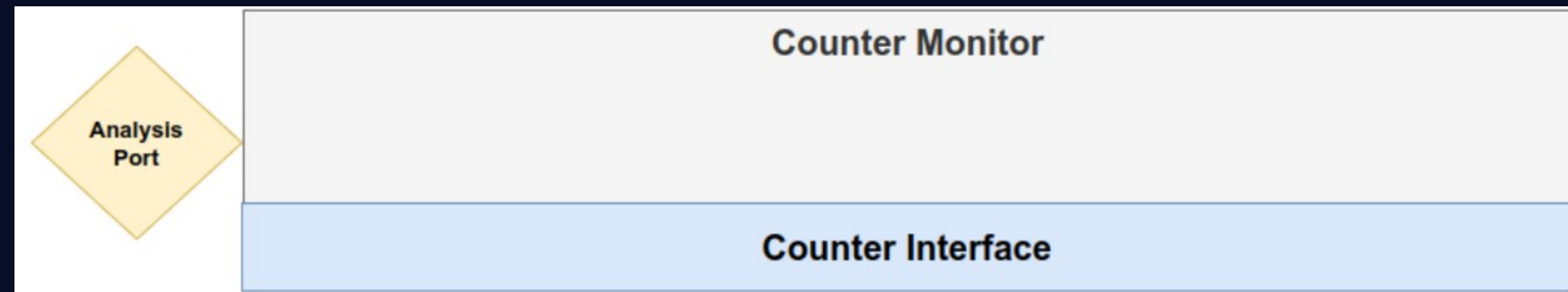
Core Functionality

- Fetch transaction from sequencer
- Decode operation & Drive Signals

UVM Monitor in UVM Testbench

Overview

- Passive component: Observes DUT behavior (no stimulus driving)
- Captures signal activity → converts to transactions
- Sends data via analysis ports for checking & analysis



Key Components

- Interface
- Sequence Item
- Analysis port

Communication Mechanism

- Uses analysis port to broadcast transactions
- Connected to:
Scoreboard
Coverage / other analysis components

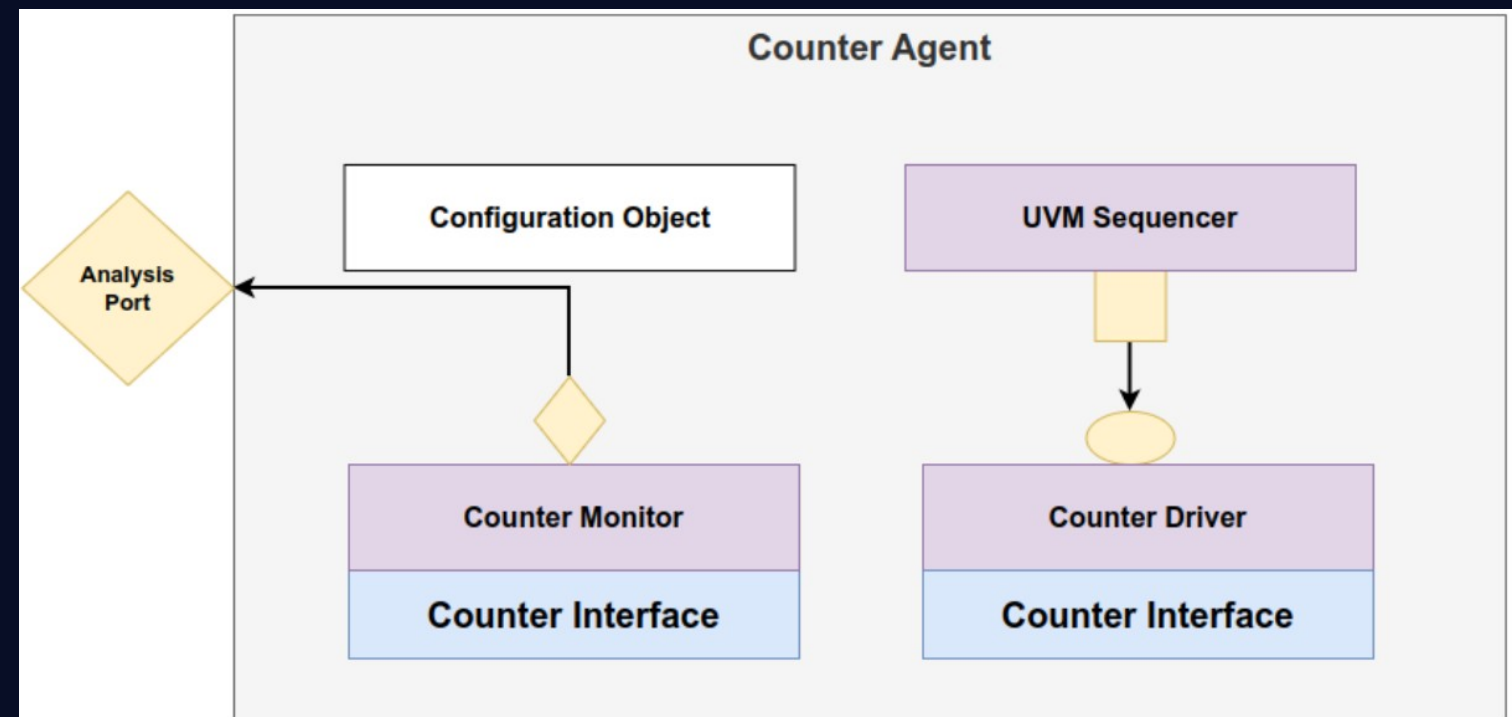
UVM Agent in UVM Testbench

Overview

- Modular component: Encapsulates Driver, Sequencer, Monitor
- Represents a complete interface-level verification unit

Key Components

- Driver
- Sequencer
- Monitor



Data Flow

- Sequencer → Driver → DUT
- DUT → Monitor → Analysis Port → Scoreboard/Predictor

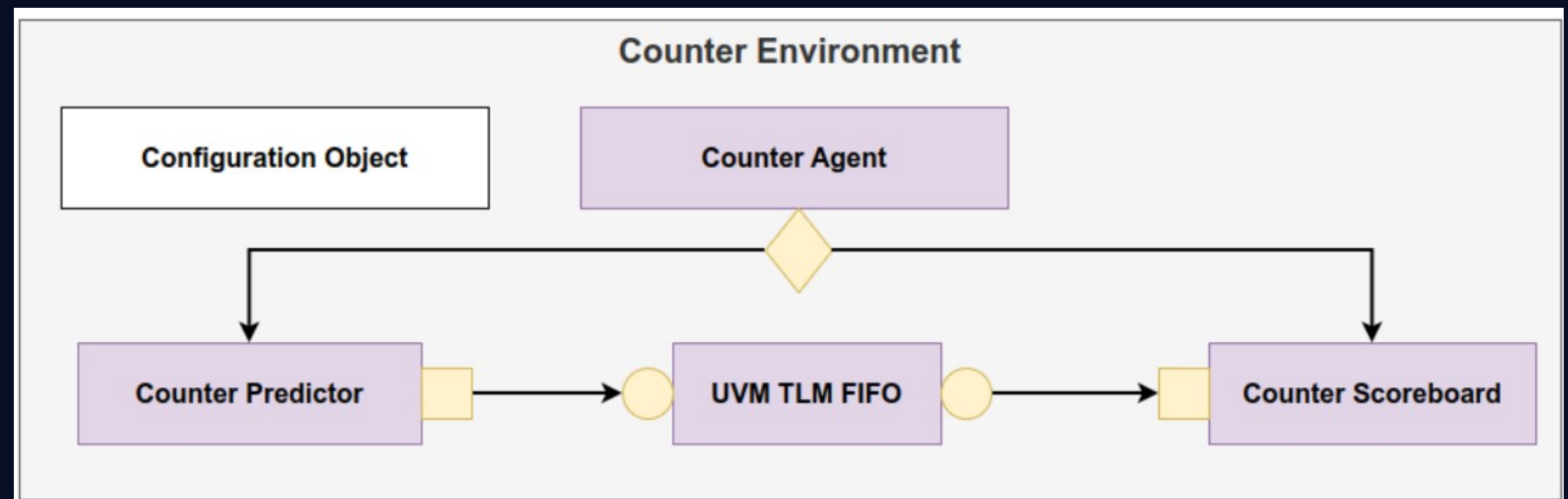
UVM Environment in UVM Testbench

Overview

- Integrates all verification components
- Manages connectivity, data flow, and coordination

Key Components

- Agent
- Predictor
- Scoreboard
- TLM FIFO



Data Flow

- Sequencer → Driver → DUT
- DUT → Monitor → Scoreboard (Actual)
- DUT → Monitor → Predictor → TLM FIFO → Scoreboard (Expected)